JXR151T User Manual

Version: V1.1

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1 Overview

The JXR151T is a high-precision, real-time clock chip with an I2C interface and a built-in 32.768KHz temperature-complementary crystal oscillator (DTCXO).

The chip has a minimum timing unit of seconds and can achieve automatic leap year correction; it can also provide timed alarm interrupt, fixed period interrupt, time update interrupt output and 32.768KHz/1024Hz/1Hz clock output.

2 Features

- Built-in high precision 32.768KHz DTCXO
- Supports high-speed I2C bus protocol (400KHz)
- Timed alarm interrupt function (settable: day of the week, day, hour, minute)
- Fixed-cycle interrupt function
- Time update interrupt function
- 32.768KHz/1024Hz/1Hz clock output with enable control
- Automatic leap year adjustment function
- Temperature compensation circuit operating voltage range: 2.2V~5.5V
- Clock circuit operating voltage range: 1.8V~5.5V
- Low current consumption: 2.2μA@3V(Typ)

3 Structure Block Diagram

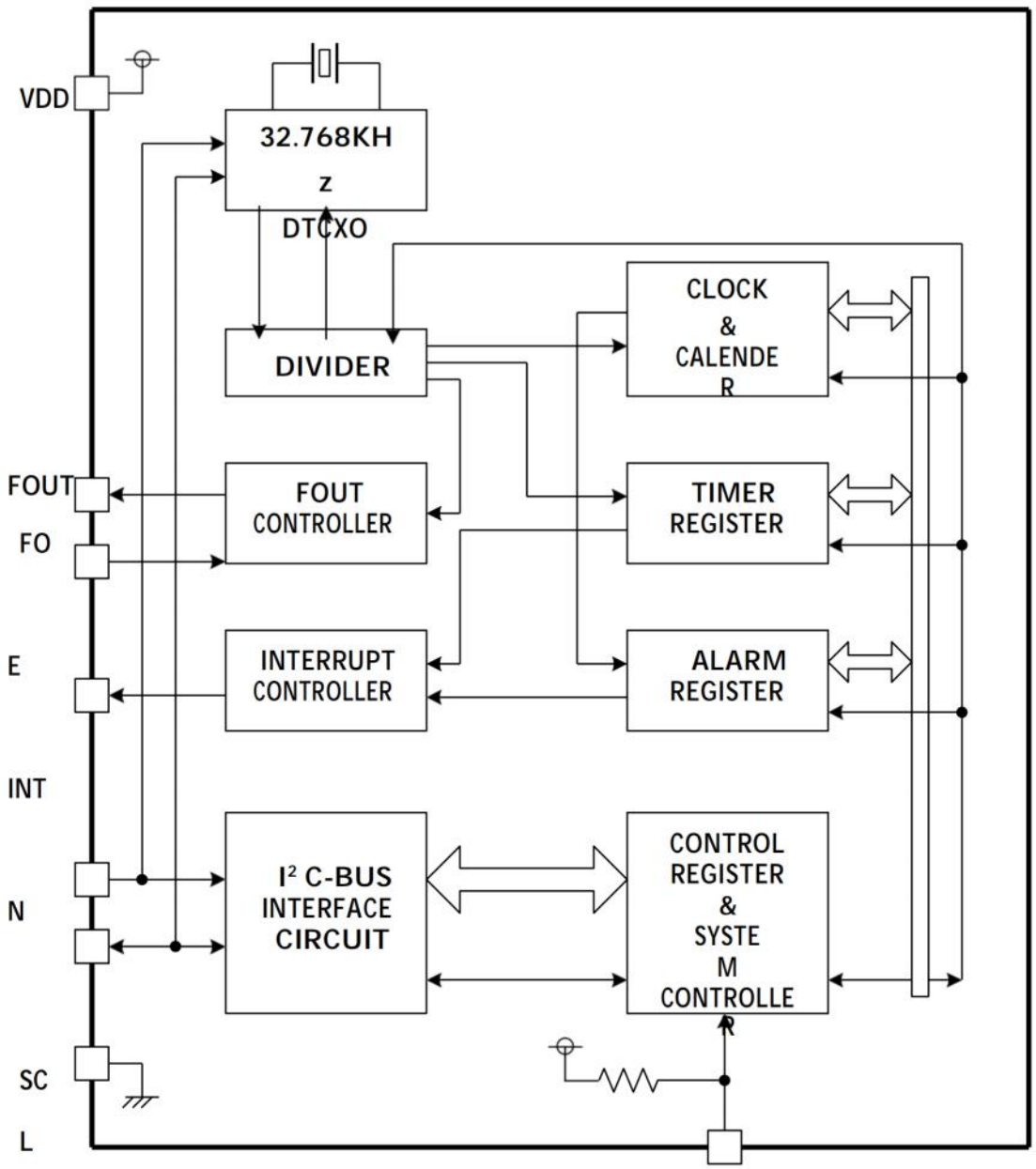


Figure 3-1 JXR151T system block diagram

4 Pin Definition

4.1 Package form

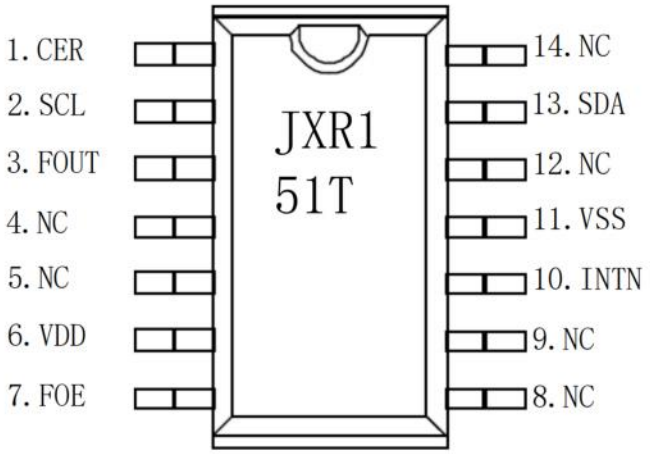


Figure 4-1 JXR151T
Package Form

4.2 Pin Function

Table 4-1 JXR151T Pin Definitions

Pin name	I/O	Function
1. CER	IN	*For factory testing (no need to connect, stay suspended)
2. SCL	IN	I^2C Serial clock input for bus communication
3. FOUT	OUT	32768Hz frequency output port, controlled via FOE, 32768Hz output when FOE=1 Clock; when FOE=0, the output is high resistance
4/5/8/9/12/14:NC	–	No connection required, stays suspended
6.VDD	POWER	Positive side of power supply
7. FOE	IN	FOUT output enable
10.INTN	OUT	Interrupt output port, N-ch open-drain output
11.VSS	GROUND	Power supply ground terminal
13.SDA	I/O	I2C bus communication data transfer terminal, N-ch open-drain output

5 Absolute electrical indicators

Table 5-1 Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Supply voltage*1	VDD	Voltage between VDD and VSS	-0.5 to 6	V
Input voltage*1, *2	VIN	FOE, SCL, SDA pins	-0.5 to VDD+0.3	V
Output voltage*1, *2	VOUT	FOUT, SDA, INTN pins	-0.5 to VDD+0.3	V
Storage temperature	TSTG	Dispersed storage, no packaging	-55 to 150	oC

*1: Each electrical indicator must not exceed the maximum rating range in the above table at any time, otherwise it will cause deterioration of relevant parameters, reliability reduction or even chip failure.

*2: Here VDD refers to the VDD range under recommended operating conditions.

6 Recommended operating conditions

Table 6-1 Recommended operating conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	Interface Voltage	1.8	3.0	5.5	V
Temperature compensated voltage	VTEM	Warm-up circuit operating voltage	2.2	3.0	5.5	V
Clock operating voltage	VCLK	Oscillator module operating voltage	1.8	3.0	5.5	V
Operating temperature	TOPR	—	-40	25	85	oC

* Any operation outside the recommended range in the above table may greatly affect the reliability of the chip.

7 Frequency characteristics

Table 7-1 Frequency Characteristics

Item	symbol	Condition	MIN	TYP	MAX	Unit
Frequency stability	Δf/f	Ta=0° C~50° C, VDD=2.2V~5V			±3.0	$\times 10^{-6}$
		Ta=-40° C~85° C, VDD=2.2V~5V			±5.0	
Voltage factor	Δf/f/V	Ta=25° C, VDD=2.2V~5.5V		±0.5	±1.0	$\times 10^{-6}$ /V

Vibration time	TSTA	Ta=25° C, VDD=1.8V			0.9	S
		Ta=-40° C~85° C, VDD=1.8V~5.5V			2.0	
Aging	fa	Ta=25° C, VDD=3.0V, first year			±1.0	$\times 10^{-6}$ /year

8 Electrical Characteristics

8.1 DC Characteristics

Table 8-1 DC Electrical Characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption	IDD1	FOE=GND FOUT=Hi-Z	VDD=5V		2.4		μA
	IDD2		VDD=3V		2.3		
Current consumption	IDD3	FOE=VDD FOUT=32.768KHz CL=0pF	VDD=5V		3.6		μA
	IDD4		VDD=3V		2.9		
Current consumption	IDD5	FOE=VDD FOUT=32.768KHz CL=30pF	VDD=5V		7.5		μA
	IDD6		VDD=3V		6.2		
High input level	VIH	CER, FOE, SCL, SDA pins	VDD=2.2V~5.5V	0.7*VDD		VDD	V
Low input level	VIL	CER, FOE, SCL, SDA pins	VDD=2.2V~5.5V	0		0.3*VDD	V
High output level	VOH	FOUT pin	IOH=-1mA	VDD-0.3		VDD	V
Low output level	VOL	FOUT, INTN pins	IOL=1mA	GND		GND+0.3	V
		SDA pin	VDD≥2V IOL=3mA	GND		GND+0.3	V
Input leakage current	ILK	FOE, SCL, SDA, $V_{IN}=V_{DD}$ or GND		-0.3		0.3	μA
Output leakage current	IOZ	INTN, FOUT, SDA, $V_{IN}=V_{DD}$ or GND		-0.3		0.3	μA

8.2 AC Characteristics

Table 8-2 AC Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	fSCL	---			400	KHz
Start condition establishment time	tSU;STA	---	0.6			μS
Starting condition holding time	tHD;STA	---	0.6			μS
Data transfer setup time	tSU;DAT	---	100			nS
Data transfer hold time	tHD;DAT	---	0		700	nS
Termination condition establishment time	tSU;STO	---	0.6			μS
Bus idle time	tBUF	Between termination condition and start condition	1.3			μS
SCL Low Time	tLOW	---	1			μS
SCL High Time	tHIGH	---	1			μS
SCL, SDA Rise time	tr	---			0.3	μS
SCL, SDA down time	tf	---			0.3	μS
Bus burr duration	tSP	---			50	nS
FOUT Output Duty Cycle	Duty	Calculated with an output of 50% of VDD	40	50	60	%

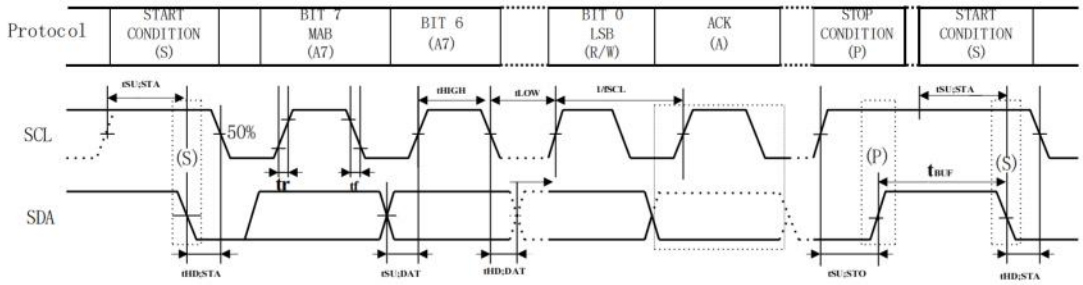


Figure 8-1 I²C Timing Legend

*I2C data transfer is located between the start condition and the end condition, the data transfer operation must be completed within 0.95S time, after which the I2C bus will be reset by the internal timer.

9 Register

9.1 Register Summary Table

Table 9-1 Register List

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	SEC	○	40	20	10	8	4	2	1
1	MIN	○	40	20	10	8	4	2	1
2	HOUR	○	○	20	10	8	4	2	1
3	WEEK	○	6	5	4	3	2	1	0
4	DAY	○	○	20	10	8	4	2	1
5	MONTH	○	○	○	10	8	4	2	1
6	YEAR	80	40	20	10	8	4	2	1
7	RAM	●	●	●	●	●	●	●	●
8	MIN Alarm	AE	40	20	10	8	4	2	1
9	HOUR Alarm	AE	●	20	10	8	4	2	1
A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
B	Timer Counter 0	128	64	32	16	8	4	2	1
C	Timer Counter 1	●	●	●	●	2048	1024	512	256
D	Extension Register	○	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET
F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET

* Make sure to write legal values to the calendar and clock registers, otherwise the chip will not perform the correct timing operation.

*The register bits marked with ○ are read-only bits and the read value is "0"; the register bits marked with ● can be used as RAM to perform read and write operations.

*If the alarm interrupt function is not set (AIE="0") registers 8~A can be used as RAM.

*If the fixed-cycle interrupt function is not set (TE=TIE="0") registers B and C can be used as RAM.

The *UF, TF, AF, VLF and VDET bits are only allowed to be written to "0".

*The CSEL0 bit is preset to "1" when the chip is powered on, FSEL1, FSEL0, CSEL1, VLF, UIE, TIE, AIE
The bit is preset to "0".

9.2 Register Details

9.2.1 Clock and calendar registers (registers 0~6)

- Data Form

  Except for the day of the week register (register 3), the data is in BCD code form. For example, the value of the seconds register is "0101 1001" means the current time is 59 seconds.

  Timing is fixed to a 24-hour format.

- Year Register and Leap Year

  The time range of the year register is from 00 to 99, and after 99, it returns to 00; when the value represented by the year register can be divided by 4, the year is judged to be a leap year; the valid period of the calendar is from 2000 to 2099.

- Day of the week register

  The day of the week register has 7 valid bits (bit0~bit6) each valid bit represents one of the days from Monday to Sunday. Therefore, only 1 bit of this register is allowed to be "1".

Table 9-2 Day of Week Register Correspondence Table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Week
0	0	0	0	0	0	1	Day
0	0	0	0	0	1	0	One
0	0	0	0	1	0	0	II
0	0	0	1	0	0	0	Three
0	0	1	0	0	0	0	IV
0	1	0	0	0	0	0	Five
1	0	0	0	0	0	0	VI

9.2.2 Alarm register (register 8~A)

The alarm can be set to X hours X minutes on X days of the week or X hours X minutes on X days of the month (weekly alarm mode and daily alarm mode). Alarm mode can be set via the WADA bit in Register D.

Each alarm register has an AE (Alarm Enable) bit (bit 7) When the AE bit of an alarm register is "0", the set value of this register needs to be compared with the corresponding timing register and the alarm interrupt is output when the value is the same; if the AE bit is "1", the corresponding alarm register value is ignored, i.e. there is no need to compare the corresponding alarm register with the timing register. If the AE bit is "1", the corresponding alarm register value is ignored, that is, there is no need to compare the corresponding alarm register with the timing register.

When selecting the week alarm mode, you can select the days of the week at the same time, i.e. WEEK ALARM in register A

Function bit0~bit6 can have several bits as "1" at the same time. Refer to Table 9-3 for the correspondence in the weekly alarm mode.

Table 9-3 Week Alarm Mode Register A Correspondence Table

Register	Function	bit6	bit5	bit4	bit3	bit2	bit1	bit0
A	Week Alarm	VI	Five	IV	Three	II	One	Day

9.2.3 Fixed cycle counter control register (register B, C)

When the value in these two registers changes from 001h to 000h, the fixed-cycle interrupt event occurs, TF is set to "1" and low is output on INTN (if TIE is "1"). "After that, the B and C registers are reset to the preset value and the countdown process starts again.

9.2.4 Control registers and flag registers (registers D~F)

- WADA Bit

  The alarm interrupt mode selection bit, when set to "1", is the daily alarm mode, when set to "0", is the weekly alarm mode.

- USEL bit

  This bit is used to set the period of the time update interrupt; it is a variable value when the chip is powered on and needs to be configured manually during use.

Table 9-4 Time Update Interrupt Mode Selection

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- TE bit

  When this position is ″1", the counter of fixed-cycle interrupt starts counting down, and when it is set to "0", it stops counting down.

- FSEL bit

  When the chip is powered on, the default value is "00".

Table 9-5 FOUT Output Frequency Selection

FSEL1	FSEL0	FOUT frequency
0	0	32.768KHz *Default
0	1	1024Hz
1	0	1Hz
1	1	32.768KHz

- TSEL bit

  Used to set the count period of a fixed-cycle interrupt.

Table 9-6 Fixed Cycle Interrupt Count Period Selection

TSEL1	TSEL0	Source clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

- AF, TF, UF bits

  The flag bits for alarm interrupt, fixed cycle interrupt and time update

interrupt are set to ″1" when the above interrupt events occur. The flag bit will remain "1" until it is manually cleared to "0", and it is prohibited to manually set the above flag bit to "1".

- AIE, TIE, UIE bit

The interrupt signal output on the INTN pin is used to set the alarm interrupt, fixed cycle interrupt, and time update interrupt events, respectively; the power-on default value of these three bits is "0".

The interrupt signal output on the INTN pin is an alarm interrupt, a fixed cycle interrupt, a logical or of a time update interrupt, and an interrupt flag bit to determine the specific interrupt situation and determine the interrupt signal output.

- VLF bit

Low voltage detection flag bit; this bit is set to "1" when the power supply voltage is detected to drop below 1.8V, causing the clock circuit to fail to operate normally, or when a power-on reset signal is detected. This flag bit will remain "1" until it is manually cleared to "0", and it is prohibited to manually set this flag bit to "1".

- VDET bit

Voltage detect flag bit; this bit is set to "1" when the supply voltage is detected to drop below 2.2V, causing the temperature compensation circuit to fail to operate normally. This flag bit will remain "1" until it is manually cleared to "0", and it is prohibited to manually set this flag bit to "1".

- CSEL bit

Used to set the time interval for the temperature compensation circuit to start; the default value is "01" (2S)after the chip is powered on.

Table 9-7 Selection of warm-up interval

CSEL1	CSEL0	Operation interval
0	0	0.5S
0	1	2S *Default
1	0	10S
1	1	30S

- RESET bit

When RESET is set to "1", the following registers are reset and the clock is stopped; the temperature compensation and VLF/VDET voltage detection functions are disabled.

The RESET bit, which is set to "1", clears to "0" in the following three cases: when an I2C termination condition is detected, when a restart condition is detected or when the I2C bus is reset after 0.95S. At the same time, the VLF/VDET flag bit is cleared to "0", resetting the supply voltage detection function.

10 Interrupt function

10.1 Alarm interruption

Alarm interruptions can be generated at set days of the week, days, hours, and minutes.

10.1.1 Alarm Interrupt Timing

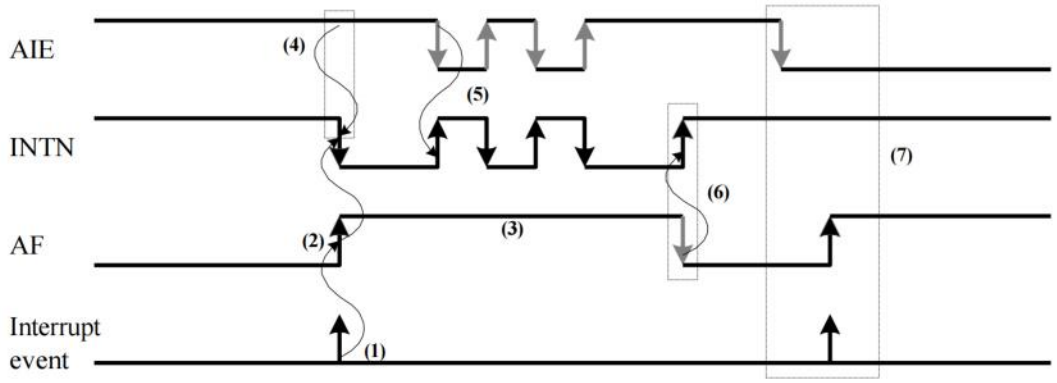


Figure 10-1 Alarm Interrupt Timing

(1) Set the hour, minute, date or week information corresponding to the alarm interrupt and the WADA register to generate an alarm interrupt event when the set time matches the current time.

(2) The AF flag bit is set to "1" when an alarm interrupt event is generated.

(3) The AF register will remain at "1" until it is manually cleared to "0".

(4) When the alarm interrupt event occurs, if AIE="1", INTN outputs low; if AIE="0", INTN remains Hi-Z
Status.

(5) If AIE is set to "0" during INTN="0", INTN reverts to Hi-Z state immediately; in case of alarm interrupt event and AF
AIE can be used to control the output state of INTN before the register is cleared to "0".

(6) Clear "0" in the AF register to clear the alarm interrupt output, and INTN will change from "0" to Hi-Z status immediately.

(7) If AIE="0" when the alarm interrupt event occurs, INTN will keep Hi-Z state and will not output low level.

10.1.2 Alarm interrupt-related registers

Table 10-1 Alarm interrupt-related registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8	MIN Alarm	**AE**	40	20	10	8	4	2	1
9	HOUR Alarm	**AE**	●	20	10	8	4	2	1
A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
D	Extension Register	○	**WADA**	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	○	○	UF	TF	**AF**	○	VLF	VDET
F	Control Register	CSEL1	CSEL0	UIE	TIE	**AIE**	○	○	RESET

- When configuring the alarm interrupt register, it is recommended to set the AIE to "0" first to prevent unnecessary hardware interrupts during operation.
- WADA is used to select the alarm mode, when set to "1", it is the daily alarm mode, when set to "0", it is the weekly alarm mode.
- The occurrence of an alarm interrupt event will set the AF flag to position "1", which will remain at "1" until manually set to "0".
- When an alarm interrupt event occurs, AIE determines whether to generate an interrupt signal output (AIE="1", then INTN="0"; AIE="0", then INTN= Hi-Z)
- If the AE bit is "0", the corresponding register needs to be compared with the clock or calendar register; if the AE bit is "1", the corresponding register is not compared, i.e., the register is always considered to match the corresponding clock or calendar register. Refer to the following example.

  (1) When register A is set to "80", only the minute alarm and hour alarm registers need to be compared with the corresponding clock registers, ignoring the day/date registers; therefore, as long as the hour and minute registers match, an alarm interrupt event will be generated for each day.

  (2) Setting the AE bits in registers 8, 9, and A to "1" will result in an alarm interrupt event once per minute.

10.2 Fixed-cycle interruptions

Fixed-cycle interrupts can generate interrupt alarm events at a fixed period between 244.14μS and 4095min.

10.2.1 Fixed Cycle Interrupt Timing

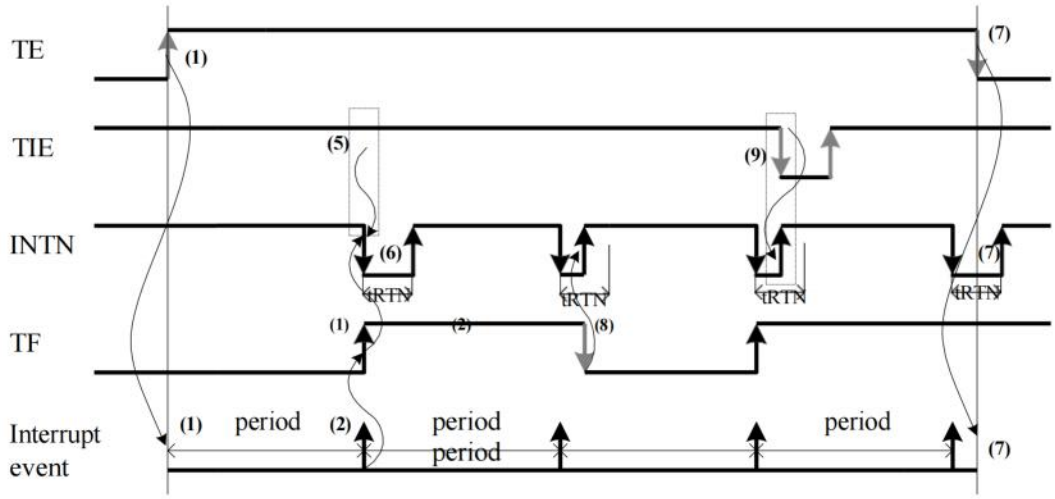


Figure 10-2 Fixed Cycle Interrupt Timing

(1) When a "1" is written to the TE bit, the fixed cycle counter counts down from the preset value.

(2) When the fixed-cycle counter counts from 001h to 000h, an interrupt event is generated; the counter is reset to the preset value and the count continues for the next time.

(3) The TF register is set to "1" when a fixed-cycle interrupt event occurs.

(4) The TF register will remain "1" until it is manually cleared to "0".

(5) When a fixed-cycle interrupt event occurs, INTN outputs low if TIE="1"; if TIE="0", INTN remains in Hi-Z state.

(6) The INTN output is low for tRTN, after which the Hi-Z state is automatically restored until the next interrupt signal is output.

(7) When TE bit is written to "0", the fixed cycle counter stops counting and INTN outputs Hi-Z (if TE write "0" occurs in
During INTN="0", after tRTN time, INTN returns to Hi-Z state)

(8) If the TF is cleared to "0" during INTN="0", the INTN reverts to Hi-Z status immediately.

(9) When the TIE is written to "0", the INTN resumes Hi-Z status immediately. If the TIE is written to 1 again during tRTN, the INTN
The Hi-Z status will still be maintained.

10.2.2 Fixed-cycle interrupt-related registers

Table 10-2 Fixed-cycle interrupt-related registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
C	Timer Counter 1	●	●	●	●	**2048**	**1024**	**512**	**256**
D	Extension Register	○	WADA	USEL	**TE**	FSEL1	FSEL0	**TSEL1**	**TSEL0**
E	Flag Register	○	○	UF	**TF**	AF	○	VLF	VDET
F	Control Register	CSEL1	CSEL0	UIE	**TIE**	AIE	○	○	RESET

- When configuring the fixed-cycle interrupt registers, it is recommended to set TE and TIE to "0" first to prevent unnecessary hardware interrupts during the operation.
- TSEL1 and TSEL0 are used to set the countdown period for fixed-cycle interrupts, and the automatic reset time of the interrupt signal on the INTN pin is related to the countdown period.

Table 10-3 Fixed Cycle Interrupt Counting Period and Auto Reset Time

TSEL1	TSEL0	Source clock	Auto reset time
0	0	4096Hz	0.122mS
0	1	64Hz	7.8125mS
1	0	1Hz	7.8125mS
1	1	1/60Hz	7.8125mS

- Register B, C set the default value of the counter (001h~FFFh). When the counter counts down to 000h with the counting period set by TSEL, a fixed-cycle interrupt event is generated.
- TE is the enable control bit of fixed-cycle counter. When TE="1", the counter starts counting down; when TE="0", the counter stops counting and terminates the fixed-cycle interrupt function.
- The occurrence of a fixed-cycle interrupt event will set the TF flag to "1", which will remain at "1" until it is manually set to "0".
- When a fixed-cycle interrupt event occurs, TIE determines whether to generate an interrupt signal output (TIE="1", then INTN="0"; TIE="0", then INTN=Hi-Z)

Table 10-4 Example of fixed-cycle interrupt period

Timer counter set value	Source clock			
	4096Hz	64Hz	1Hz	1/60Hz
0	—	—	—	—
1	244.14μS	15.625mS	1S	1min
.....	.....	.....	.....	.....

2048	500mS	32S	2048S	2048min
.....	.....	.....	.....	.....
4095	0.9998S	63.984S	4095S	4095min

10.3 Time update interruption

Depending on the set value, the time update interrupt generates an interrupt alarm event in seconds update or minutes update.

10.3.1 Time Update Interrupt Timing

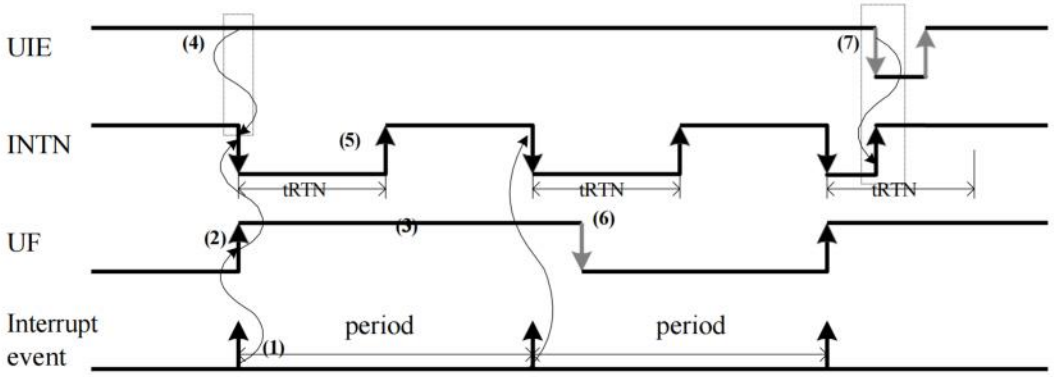


Figure 10-3 Time Update Interrupt Timing

(1) The USEL register determines whether the chip is in a second update interrupt or a minute update interrupt state, and generates a time update interrupt event when the corresponding second register or minute register is updated.

(2) When the time update interrupt event is generated, the UF register is set to "1".

(3) The UF register will remain "1" until it is manually cleared to "0".

(4) When the time update interrupt event occurs, if UIE="1", INTN outputs low; if UIE="0", INTN remains as
Hi-Z status.

(5) The INTN output is low for tRTN, after which the Hi-Z state is automatically restored until the next interrupt signal is output.

(6) If the UF is cleared to "0" during INTN="0", the Hi-Z state of the INTN is restored after the tRTN time.

(7) If UIE is set to "0" during INTN="0", INTN resumes Hi-Z state immediately and the interrupt signal output ends. If tRTN
If the UIE is written to 1 again during this period, the INTN will remain in the Hi-Z state.

10.3.2 Time update interrupt-related registers

Table 10-5 Time Update Interrupt-Related Registers

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D	Extension Register	○	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
E	Flag Register	○	○	**UF**	TF	AF	○	VLF	VDET
F	Control Register	CSEL1	CSEL0	**UIE**	TIE	AIE	○	○	RESET

- When configuring the time update interrupt register, it is recommended to set UIE to "0" first to prevent unnecessary hardware interrupts during the operation.
- The USEL signal is used to set the interrupt mode to second update or minute update.

Table 10-6 Time Update Interrupt Mode

USEL	Timing	Auto return time
0	1Hz	500ms
1	1/60Hz	7.81ms

- The occurrence of a time update interrupt event will place the UF flag at "1" and the bit will remain at "1" until it is manually cleared to "0".
- When a time update interrupt event occurs, UIE determines whether to generate an interrupt signal output (UIE="1", then INTN="0"; UIE="0", then INTN=Hi-Z)

11 I2C bus interface

11.1 I2C Bus Features

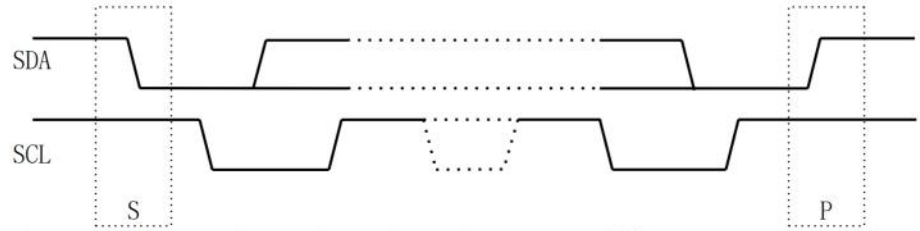
I2C is a bi-directional communication interface with the signal line SDA and clock line SCL connected to VDD via pull-up resistors; the port connected to the I2C bus must be open-drain in order to enable multi-device line and connection.

11.2 Data Transfer

Each SCL clock cycle can transmit 1 bit of data. When sending data, the data on the SDA line changes during the SCL low level; when receiving data, stable and valid data can be obtained from the data line SDA during the SCL high level.

11.3 Start and end conditions

During the idle state, SCL and SDA are held high, and the falling edge of SDA is used as the start condition for I2C communication when SCL is high, and the



rising edge of SDA is used as the end condition for I2C communication when SCL is high.

Figure 11-1 I²C Start and End Conditions

11.4 Device selection (from address)

I2C bus devices have no chip select signal, the master device selects the corresponding slave device by sending a unique fixed device number (slave address), and the selected slave device sends an answer signal to establish communication with the master device.

The slave address of the JXR151T is "0110010", which includes 7 bits of data, 4 bits (Group 1) + 3 bits (Group 2). During communication, the slave address and the R/W selection bit are sent as 8bit data.

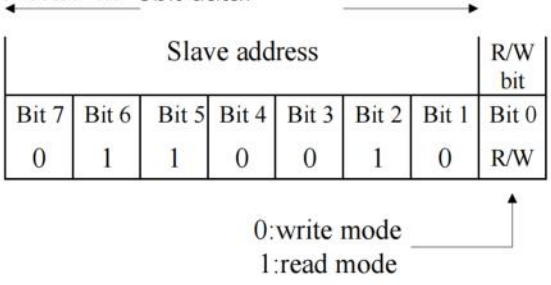


Figure 11-2 I²C from address schematic

11.5 System Configuration

The device that controls data transmission is called "master device", and the device controlled by the master device is called "slave device"; the device that sends data is called "sender", and the device that receives data is called "receiver". is called "receiver".

In the JXR151T system, the CPU or other control device is the master device and the JXR151T chip itself is the slave device; both the master and slave devices can be used as the transmitter or receiver.

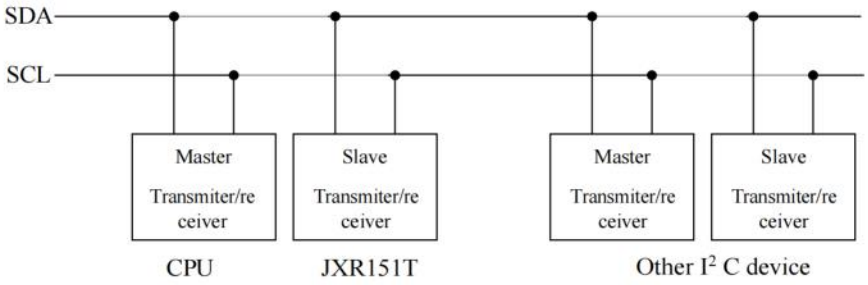


Figure 11-3 I² C System Configuration

11.6 Answer Signal

There is no limit to the number of bytes that can be transferred between the start and end conditions on the I2C bus. After each byte of data has been transferred, the transmitter has to release the SDA bus and provide 1 SCL clock to receive the answer signal. If the receiver succeeds in receiving 8 bits of data, the SDA must be set to "0" after the last 1 bit of data has been transferred and the transmitter will use this low level as an answer signal for successful data transfer; after one clock cycle, the receiver releases the SDA bus and is ready to receive new data.

The I2C bus terminates data transfer when the following conditions are met.

(1) When the master device acts as the sender, it sends the termination condition after receiving the answer signal from the slave device.

(2) When the master device is the receiver, it sends a "1" as an answer signal after successfully receiving 8 bits of data and then sends an abort condition.

11.7 I2C bus control

This section describes the I2C bus communication timing for the CPU as the master device and the JXR151T as the slave device.

11.7.1 Specified address write operation

JXR151T has an automatic address increment function. After setting the operation address, you only need to send data continuously and the address bits can be incremented automatically.

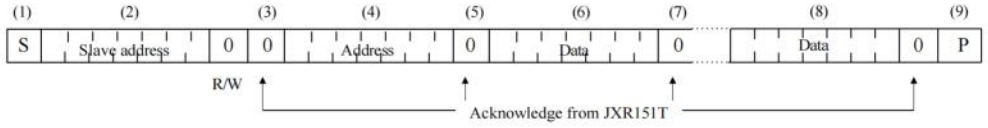


Figure 11-4 Specified Address Write Operation

(1) The CPU sends the start condition [S].

(2) The CPU sends the JXR151T from the address and sets it to write mode via the R/W bit.

(3) The JXR151T generates an answer signal.

(4) CPU sends write register address to JXR151T.

(5) The JXR151T generates an answer signal.

(6) The CPU sends data to the register corresponding to the address specified in (4).

(7) The JXR151T generates an answer signal.

(8) Repeat the process of (6)(7), the address of the write register in JXR151T will be incremented automatically.

(9) The CPU sends the termination condition [P].

11.7.2 Specified address read operation

After writing to the register, the CPU can read the register data by setting the read mode.

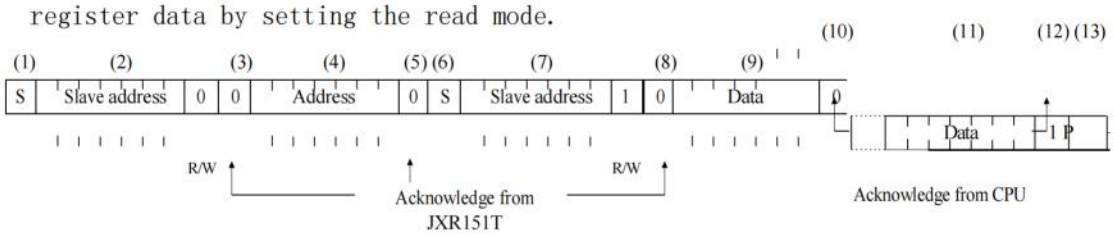


Figure 11-5 Specified Address Read Operation

(1) The CPU sends the start condition [S].

(2) The CPU sends the JXR151T from the address and sets it to write mode via the R/W bit.

(3) The JXR151T generates an answer signal.

(4) CPU sends read register address to JXR151T.

(5) The JXR151T generates an answer signal.

(6) The CPU resends the start condition.

(7) The CPU sends the JXR151T from the address and sets it to read mode via the R/W bit.

(8) The JXR151T generates an answer signal; after that, the CPU acts as the receiver and the JXR151T acts as the sender.

(9) JXR151T sends the data in the register corresponding to the address specified in (4).

(10) The CPU sends an answer signal to the JXR151T.

(11) Repeat the process of (9) (10), the address of the read register in JXR151T will be incremented automatically.

(12) The CPU sends an answer signal to the JXR151T.

(13) The CPU sends the termination condition [P].

11.7.3 Unassigned address read operation

The master device directly enters the read mode to read the contents of all registers in the slave device. If the operation is preceded by a read operation, the read operation continues from the address of the register already read + 1; if the operation is preceded by a write operation, the read operation starts from the first register address corresponding to the write operation.

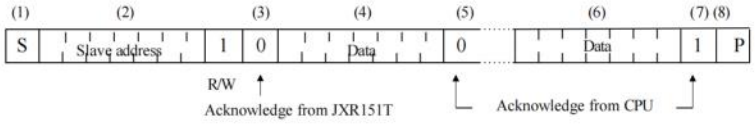


Figure 11-6 Unassigned Address Read Operation

(1) The CPU sends the start condition [S].

(2) The CPU sends the JXR151T from the address and sets it to read mode via the R/W bit.

(3) The JXR151T generates an answer signal; after that, the CPU acts as the receiver and the JXR151T acts as the sender.

(4) JXR151T automatically increments the register address and sends the register data.

(5) The CPU sends an answer signal to the JXR151T.

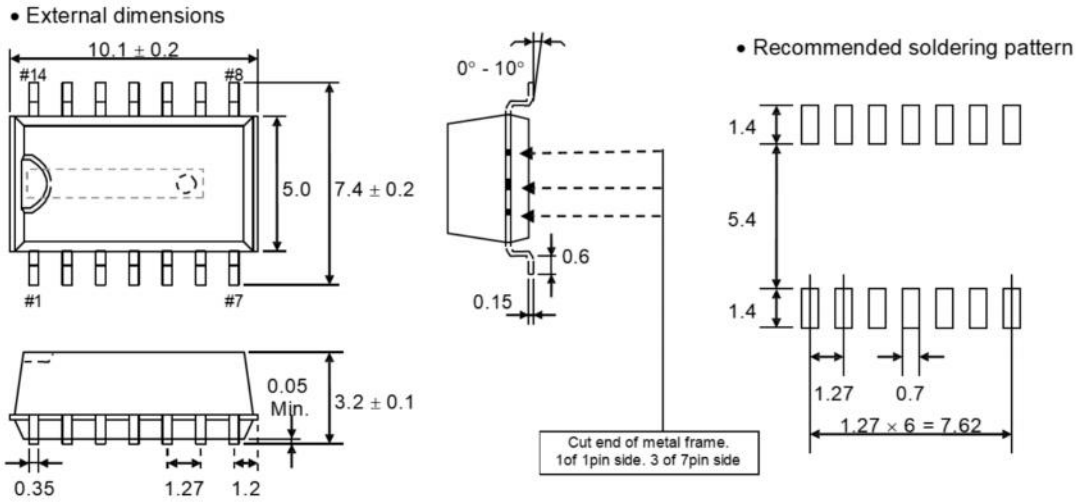
(6) Repeat the process of (4) (5), the address of the read register in JXR151T will be incremented automatically.

(7) The CPU sends an answer signal to the JXR151T.

(8) The CPU sends the termination condition [P].

Appendix

Package Size

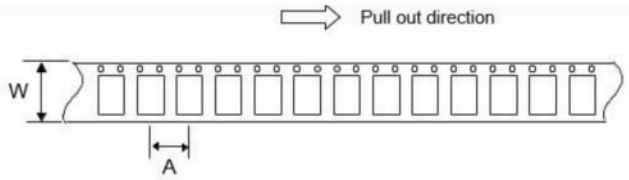


Package specification

SOP Emboss Taping (TE2)

Symbol	SOP14
A	8
W	16

Unit : mm



Symbol	SOP14
A	330
W	16.4
Contents	1000 pcs

Unit : mm