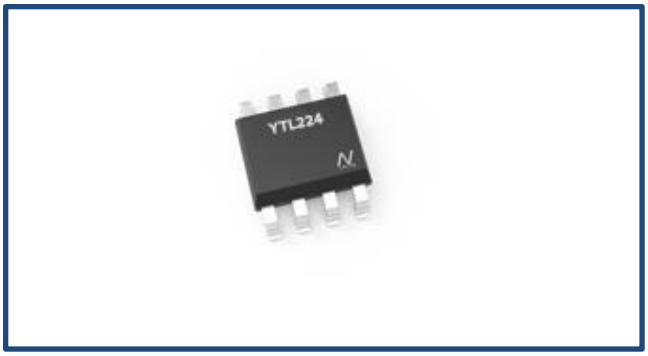
YTL224

High Reliability Dual-Channel Digital Isolators

Datasheet (EN) 1.0

Product Overview

YTL224 is a high reliability dual-channel digital isolator. The YTL224 device is safety certified by UL1577 support 3kV$_{rms}$ insulation withstand voltages(>4.5kV$_{rms}$ in Oil), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the YTL224 is up to 500kbps, and the common-mode transient immunity (CMTI) is up to 100kV/us. The YTL224 device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the YTL224 device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.



Key Features

- Up to 3000V$_{rms}$ Insulation voltage, (>4500V$_{rms}$ in Oil)
- Date rate: DC to 500kbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 100kV/us
- Chip level ESD: HBM: ±6kV
- High system level EMC performance:
  Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low level option
- Isolation barrier life: >60 years
- Low power consumption: 1mA/ch (500kbps)
- Propagation delay: <500ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  SOIC-8 narrow body

Safety Regulatory Approvals

- UL recognition: up to 3000V$_{rms}$ for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Functional Block Diagrams

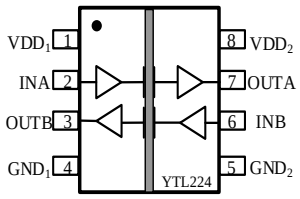


Figure 1. YTL224 Block Diagram

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1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB	-0.4		VDD+0.4[1]	V	
Maximum Output Voltage	V_{OUTA}, V_{OUTB}	-0.4		VDD+0.4[1]	V	
Maximum Input/Output Pulse Voltage	VINA, VINB, V_{OUTA}, V_{OUTB}	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Common-Mode Transients	CMTI			±100	kV/us	
Output current	Io	-15		15	mA	
Maximum Surge Isolation Voltage	V_{IOSM}			5.3	kV	
Operating Temperature	Topr	-40		125	℃	
Storage Temperature	Tstg	-40		150	℃	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

[1] The maximum voltage must not exceed 6.5V.

2.0 SPECIFICATIONS

2.1. ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
High Level Input Voltage	V_{IH}	0.7*VDD			V	
Low Level Input Voltage	V_{IL}			0.3*VDD	V	
High Level Output Voltage	V_{OH}	VDD-0.3			V	I_{OH} ≤ 4mA
Low Level Output Voltage	V_{OL}			0.3	V	I_{OL} ≤ 4mA
Output Impedance	R_{out}		50		ohm	

Input Pull high or low Current	I_{pull}		8	15	uA	
Start Up Time after POR	trbs		40		usec	
Common Mode Transient Immunity	CMTI	±80		±100	kV/us	

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	YTL224					
	I_{DD1}(Q0)		0.8		mA	All Input 0V for YTL224x0 Or All Input at supply for YTL224x1
	I_{DD2}(Q0)		0.8		mA	
	I_{DD1}(Q1)		1.4		mA	All Input at supply for YTL224x0 Or All Input 0V for YTL224x1
	I_{DD2}(Q1)		1.4		mA	
	I_{DD1}(0.5M)		1.25		mA	All Input with 500kbps, C_L=15pF
	I_{DD2}(0.5M)		1.25		mA	
Data Rate	DR	0		0.5	Mbps	
Minimum Pulse Width	PW			500.0	ns	
Propagation Delay	t_{PLH}		440		ns	See Figure 2.7 , C_L = 15pF
	t_{PHL}		440		ns	See Figure 2.7, C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			10.0	ns	See Figure 2.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 2.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 2.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			10.0	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			10.0	ns	

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	YTL224					
	I_{DD1}(Q0)		0.77		mA	All Input 0V for YTL224x0 Or All Input at supply for YTL224x1
	I_{DD2}(Q0)		0.77		mA	
	I_{DD1}(Q1)		1.35		mA	All Input at supply for YTL224x0 Or All Input 0V for YTL224x1
	I_{DD2}(Q1)		1.35		mA	
	I_{DD1}(0.5M)		1.11		mA	All Input with 500kbps, C_L = 15pF
	I_{DD2}(0.5M)		1.11		mA	
Data Rate	DR	0		0.5	Mbps	
Minimum Pulse Width	PW			500.0	ns	
Propagation Delay	t_{PLH}		440		ns	See Figure 2.7 , C_L = 15pF
	t_{PHL}		440		ns	See Figure 2.7, C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			10.0	ns	See Figure 2.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 2.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 2.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			10.0	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			10.0	ns	

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	**YTL224**					
	I_{DD1}(Q0)		0.75		mA	All Input 0V for YTL224x0 Or All Input at supply for YTL224x1
	I_{DD2}(Q0)		0.75		mA	
	I_{DD1}(Q1)		1.33		mA	All Input at supply for YTL224x0 Or All Input 0V for YTL224x1
	I_{DD2}(Q1)		1.33		mA	
	I_{DD1}(0.5M)		1.08		mA	All Input with 500kbps, C_L = 15pF
	I_{DD2}(0.5M)		1.08		mA	
Data Rate	DR	0		0.5	Mbps	
Minimum Pulse Width	PW			500.0	ns	
Propagation Delay	t_{PLH}		440		ns	See Figure 2.7 , C_L = 15pF
	t_{PHL}		440		ns	See Figure 2.7, C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			10.0	ns	See Figure 2.7 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 2.7 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 2.7 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			10.0	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

2.2. PARAMETER MEASUREMENT INFORMATION

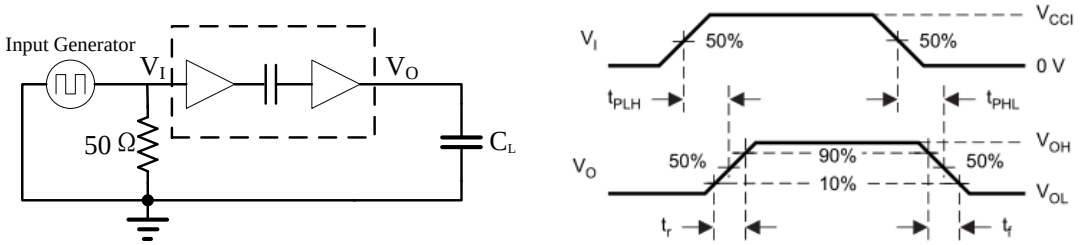


Figure 2.7 Switching Characteristics Test Circuit and Waveform

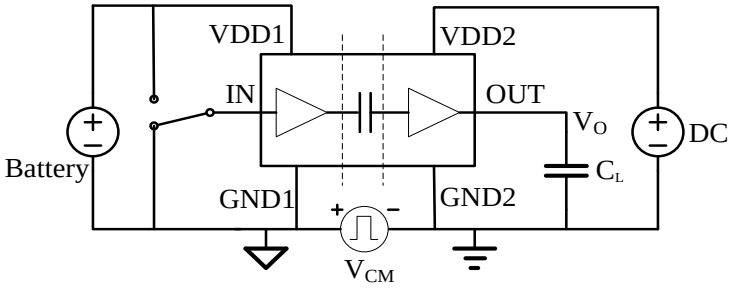


Figure 2.8 Common-Mode Transient Immunity Test Circuit

3.0 HIGH VOLTAGE FEATURE DESCRIPTION

3.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

Parameters	*Symbol*	*Value* *SOIC-8*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	L(I01)	4.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20	um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>400	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		Ⅱ		

3.2. DIN VDE V 0884-11（VDE V 0884-11）:2017-01 INSULATION CHARATERISTICS

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
			SOIC-8	
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150V_{rms}			Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 300V_{rms}			Ⅰ to Ⅲ	
For Rated Mains Voltage ≤ 400V_{rms}			Ⅰ to Ⅲ	
Climatic Classification			10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive isolation voltage		VIORM	565	Vpeak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	847	Vpeak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	Vpeak
Maximum transient isolation voltage	t = 60 sec	VIOTM	5300	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, VTEST=VIOSM×1.3	VIOSM	5384	Vpeak
Isolation resistance	VIO =500V	RIO	>10^9	Ω
Isolation capacitance	f = 1MHz	CIO	0.6	pF
Input capacitance		CI	2	pF
Total Power Dissipation at 25℃		Ps		mW
Safety input, output, or supply current	θJA = 140 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C	Is	160	mA
	θJA = 84 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C			mA
Case Temperature		Ts	150	℃

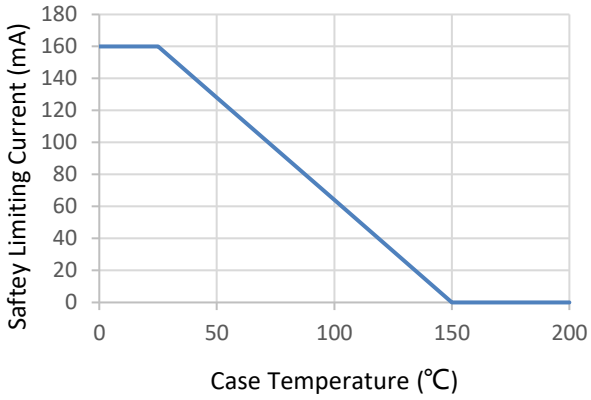


Figure 3.1 YTL224 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

3.3. REGULATORY INFORMATION

The YTL224 are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3000V_{rms} Isolation voltage	Single Protection, 3000V_{rms} Isolation voltage	Basic Insulation 565Vpeak, V_{IOSM}=5384Vpeak	Basic insulation at 400V_{rms} (565Vpeak)
File (E500602)	File (E500602)	File (5024579-4880-0001)	File (pending)

[1] In accordance with UL 1577, each YTL224 is proof tested by applying an insulation test voltage ≥ 3600 V_{rms} for 1 sec.

[2] In accordance with DIN VDE V 0884-11, each YTL224 is proof tested by applying an insulation test voltage ≥ 847 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

4.0 FUNCTION DESCRIPTION

The YTL224 is Dual-channel digital isolators based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The YTL224 devices is high reliability dual-channel digital isolator. The YTL224 device is safety certified by UL1577 support 3kV$_{rms}$ insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the YTL224 is up to 500kbps, and the common-mode transient immunity (CMTI) is up to 100kV/us. The YTL224 device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the YTL224 device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The YTL224 has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 4.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 1us after powering up.

Table 4.1 Output status vs. power status

Input	*VDD1 status*	*VDD2 status*	*Output*	*Comment*
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L(YTL224N0) H(YTL224N1)	The output follows the same status with the input within 60us after input side VDD1 is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 60us after output side VDD2 is powered on.

5.0 APPLICATION NOTE

5.1. PCB LAYOUT

The YTL224 requires a 0.1 µF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 5.1 to Figure 5.4 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

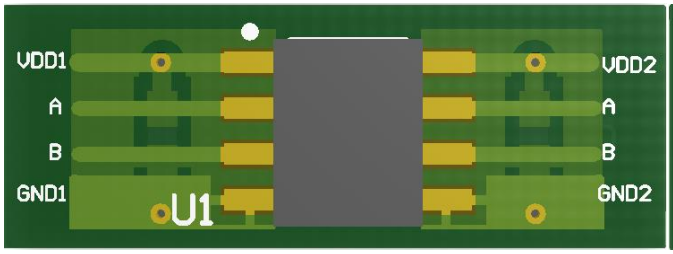


Figure5.1 Recommended PCB Layout — Top Layer

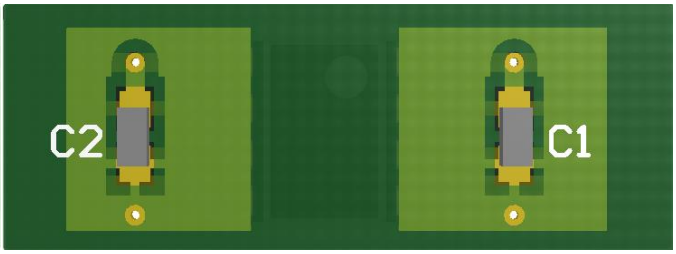


Figure5.2 Recommended PCB Layout — Bottom Layer

6.0 PACKAGE INFORMATION

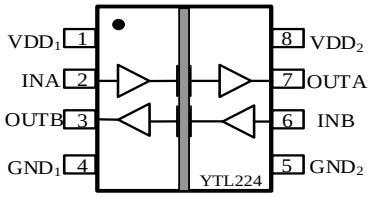


Figure 6.2 YTL224 Package

Table6.1 YTL224 Pin Configuration and Description

YTL224 PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD1	Power Supply for Isolator Side 1
2	INA	Logic Input A
6	INB	Logic Input B
4	GND1	Ground 1, the ground reference for Isolator Side 1
5	GND2	Ground 2, the ground reference for Isolator Side 2
3	OUTB	Logic Output B
7	OUTA	Logic Output A
8	VDD2	Power Supply for Isolator Side 2

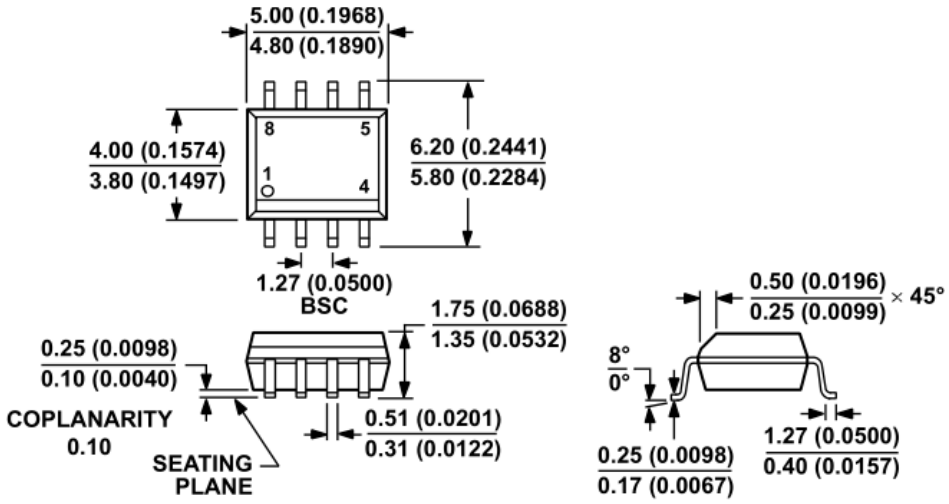
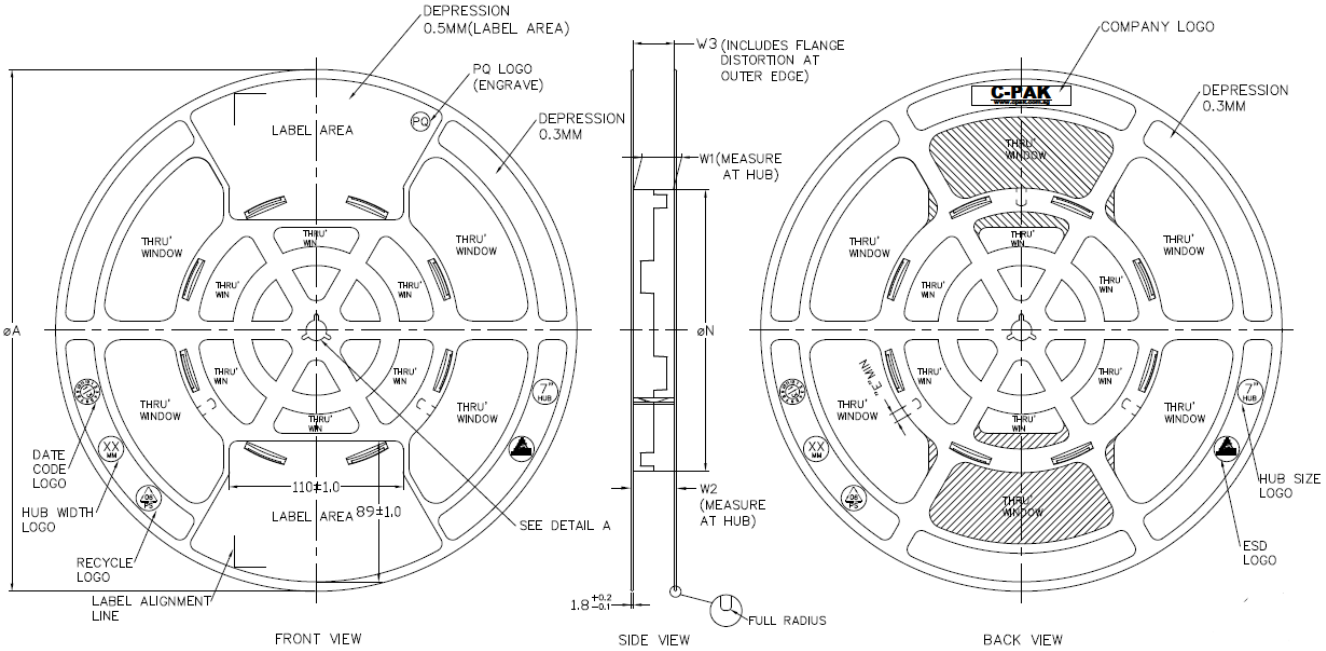
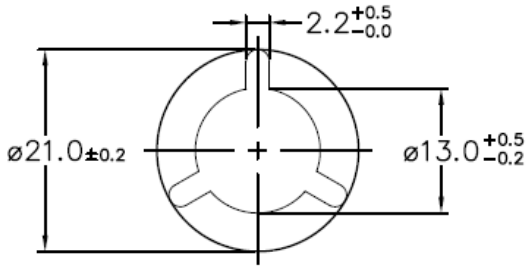


Figure 6.3 SOIC8 Package Shape and Dimension in millimeters (inches)

7.0 TAPE AND REEL INFORMATION

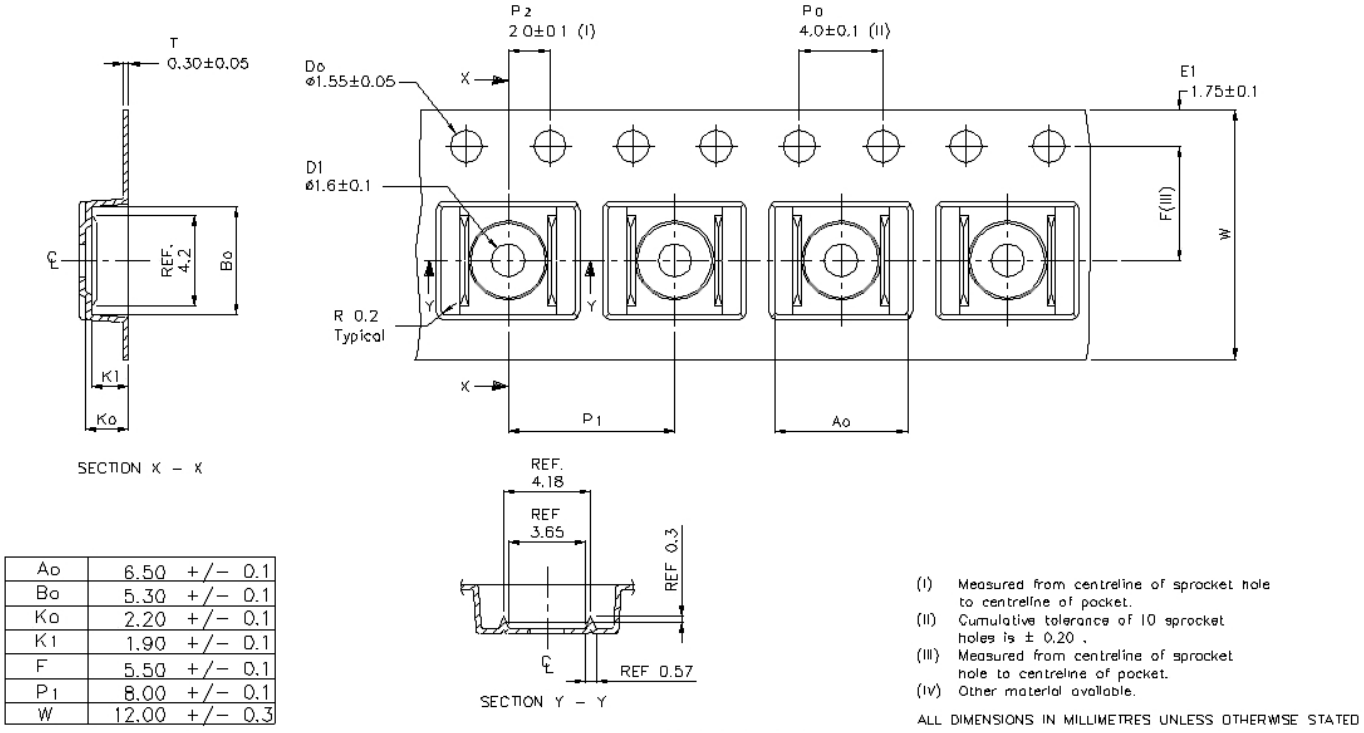




ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{8} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



Ao	6.50 +/– 0.1
Bo	5.30 +/– 0.1
Ko	2.20 +/– 0.1
K1	1.90 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 7.1 Tape and Reel Information of SOIC8

8.0 ORDER INFORMATION

Part Number Rule:

Part No.	*Isolation Rating(kV)*	*Number of side 1 inputs*	*Number of side 2 inputs*	*Max Data Rate (Mbps)*	*Default Output State*	*Temperature*	*SPQ*	*Package*
YTL224-DSPR	3	1	1	0.5	High	-40 to 125℃	2500	SOIC8
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.								

9.0 REVISION HISTORY

Revision	Description	Date
1.0	Original	2020/6/22